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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/190,208	11/13/1998	JIASHU CHEN	CHEN3-1	6397

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EXAMINER

LAO, LUN S

ART UNIT PAPER NUMBER

2644

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/190,208

Applicant(s)

CHEN ET AL.

Examiner

Lun-See Lao

Art Unit

2644

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15-49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 15-49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Introduction

1. The request filed on 07-05-2005 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/190,208 is acceptable and a CPA has been established. An action on the CPA follows.
2. This action is in response to the amendment filed on 07-05-2005. Claims 1-14 have been canceled and claims 15-49 have been added. Claims 15-49 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 15-17, 19, 21-23, 25-30, 32-35 and 37, 39, 41-46, 48-49 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagata et al. (US PAT. 5,974,154).

Consider claim 15 Nagata teaches that an apparatus for generating a delayed output digital audio signal from an input digital audio signal, the apparatus comprising:

a first delay module (see fig.2, (61)) adapted to apply a first amount of delay to the input digital audio signal to generate a partially delayed digital audio signal, wherein the first delay module is adapted to select the first amount of delay from a plurality of

available first delay values separated from one another by increments at a first resolution level (see col. 4 line 60-col.5 line 23); and

a second delay module (71) adapted to apply a second amount of delay to the partially delayed digital audio signal to generate the delayed output digital audio signal, wherein the second delay module is adapted to select the second amount of delay from a plurality of available second delay values separated from one another by increments at a second resolution level different from the first resolution level (it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 4 line 60-col.5 line 67).

Consider claim 33, there is the method claim corresponding to apparatus claim 15. See previous apparatus claim 15 rejection.

Consider claims 16-17 and 34-35, Nagata teaches that the total range of the plurality of available second delay values at the second resolution level is substantially equal to each increment at the first resolution level (it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 4 line 60-col.5 line 67); and the first delay module (see fig.2, 61) comprises:

a buffer (such as RAM) adapted to receive and store a plurality of digital values corresponding to the input digital audio signal such that each position in the buffer corresponds to a different one of the plurality of available first delay values (see co.4 line 40-col.5 line 44); and

a switch (45) having a plurality of input ports and an output port, wherein:

Art Unit: 2644

each input port is connected to receive a different digital value stored in the buffer (66); and the switch (45) is adapted to present one of the received digital values at its output port based on a first delay (61) control signal.

Consider claims 19 and 37, Nagata teaches that the second delay module (see fig.2, 71) comprises:

a plurality of digital filters (see fig.2, 73R1-73Rn and 73L1-73Ln), configured in parallel, each digital filter adapted to apply a different one of the plurality of available second delay values; and switch circuitry (45) adapted to select, based on a second delay control signal, one of the digital filters (see fig.2, 73R1-73Rn and 73L1-73Ln) to provide the second amount of delay (71 and it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 4 line 60-col.5 line 67).

Consider claims 21-23 and 39, Nagata teaches that the switch circuitry (see fig.2, multipliers 621-62n, 45, 50) comprises an input switch adapted to receive and forward the partially delayed digital audio signal (see fig.2, TD1-TDn) to only the selected digital filter (see col. 4 line 60-col.5 line67); and the switch circuitry (see fig.2, multipliers 621-62n, 45, 50) further comprises an output multiplexer having a plurality of input ports and an output port, wherein: each input port is connected to a different digital filter; and the output multiplexer (see fig.2, multipliers 621-62n) is adapted to present the output from the selected digital filter at its output port (see col. 4 line 60-col.5 line67); and a control module (see fig.2, 65, microcomputer) adapted to generate first and second delay

Art Unit: 2644

(61,71) control signals used by the first and second delay modules to select the first and second amounts of delay (see col. 5 line 10-col. 6 line 61).

Consider claims 25-29 and 41-45, Nagata teaches that the first delay module (see fig.2, 61) is a coarse delay module having a coarse resolution level; and the second delay module (71) is a fine delay module having a fine resolution level that is finer than the coarse resolution level (it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 4 line 60-col.5 line 67); and the first and second amounts of delay (see fig.2, (61,71)) are applied to the input digital audio signal to create a relative delay between the delayed output digital audio signal and a second digital audio signal (see col. 4 line 60-col.5 line 67); and the delayed output and second digital audio signals are left and right ear signals (see fig.2, 74R and 74L); and the coarse delay module is adapted to generate the second digital audio signal by delaying the input digital audio signal by a coarse delay value (it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 4 line 60-col.5 line 67); and the coarse delay value used to generate the second digital audio signal is different from the first amount of delay used to generate the partially delayed digital audio signal (it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 4 line 60-col.5 line 67).

Consider claims 30 and 46, Nagata teaches that that a control module (see fig.2, 65, microcomputer) adapted to generate first and second delay control signals used by the

Art Unit: 2644

first and second delay modules to select the first and second amounts of delay, wherein:

the first delay module (see fig.2, 61) comprises: a buffer (61, RAM) adapted to receive and store a plurality of digital values corresponding to the input digital audio signal such that each position in the buffer corresponds to a different one of the plurality of available first delay values (see col.4 line 42-col. 6 line 10); and a switch (45,50) having a plurality of input ports and an output port wherein: each input port is connected to receive a different digital value stored in the buffer (66); and the switch (45,50) is adapted to present one of the received digital values at its output port based on the first delay control signal (col. 5 line 45-col. 6 line 61); the second delay module (71) comprises: a plurality of digital filters (73R1-73RI and 73L1-73Ln), configured in parallel, each digital filter adapted to apply a different one of the plurality of available second delay values; and switch circuitry (45, 50) adapted to select, based on the second delay control signal, one of the digital filters to provide the second amount of delay; and the total range of the plurality of available second delay values at the second resolution level is substantially equal to each increment at the first resolution level (it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 4 line 60-col.5 line 67).

Consider claims 32 and 48, Nagata teaches that the first delay module (see fig. 2, 61) is a coarse delay module having a coarse resolution the second delay module is a fine delay module having a fine resolution level that is finer than the coarse resolution level;

the first and second amounts of delay (61,71) are applied to the input digital audio signal to create a relative delay between the delayed output digital audio signal and a second digital audio signal (see col. 4 line 42-col.5 line 67);

the delayed output and second digital audio signals are left and right ear signals (74L, 74R);

the coarse delay module is adapted to generate the second digital audio signal by delaying the input digital audio signal by a coarse delay value; the coarse delay value used to generate the second digital audio signal is different from the first amount of delay used to generate the partially delayed digital audio signal (it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 5 line 10-col.6 line 61).

Consider claim 49, Nagata teaches that an apparatus for generating a delayed output digital audio signal from an input digital audio signal, the apparatus comprising:

- (a) means (see fig.2, 61) for applying a first amount of delay to the input digital audio signal to generate a partially delayed digital audio signal, wherein the first amount of delay is selected from a plurality of available first delay values separated from one another by increments at a first resolution level; and
- (b) means (71) for applying a second amount of delay to the partially delayed digital audio signal to generate the delayed output digital audio signal, wherein the second amount of delay is selected from a plurality of available second delay values separated from one another by increments at a second resolution level different from the first

Art Unit: 2644

resolution level (it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 4 line 60-col.5 line 67).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 18 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata (US PAT. 5,974,154) in view of Platt (US PAT. 5,337,363).

Consider claims 18 and 36, Nagata does not clearly teaches that the buffer is a first-in, first-out (FIFO) buffer adapted to receive a new digital value in the input digital audio signal at each clock cycle of the FIFO buffer.

However, Platt teaches that the buffer is a first-in, first-out (FIFO) buffer adapted to receive a new digital value in the input digital audio signal at each clock cycle of the FIFO buffer (see col.9 line 20-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Platt in to Nagata to produce the sound being generated on a real time basis.

7. Claims 20 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata (US PAT. 5,974,154) in view of Gerzon (US PAT. 5,671,287).

Art Unit: 2644

Consider claims 20 and 38, Nagata and Platt do not clearly teach that the digital filters are all-pass filters having different phase shift values.

However, Gerzon teaches that the digital filters are all-pass filters having different phase shift values (see figs 23a-23c and col. 33 line 25-col. 34 line 48 and col. 42 line 5-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Gerzon into the teaching of Nagata to provide a pseudostereo or directional dispersion effect with both low phasiness and a substantially flat reproduced total energy response.

Claims 24 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata (US PAT. 5,974,154) in view of Myers (US PAT. 4,817,149).

Consider claims 24 and 40, Nagata teaches that the control module comprises a look-up table (LUT) (see fig.4) storing data that maps 3D positions to time delays; and the control module is adapted to: receive a specified 3D position value; retrieve a corresponding time delay value from the LUT based on the specified 3D position value (see col.6 line 7-col. 7 line 27); and generate the first and second delay control signals on the retrieved time delay value (see fig.2 and col. 4 line 60-col. 5 line 67); but Nagata fails to teach an interaural delay value.

Mayer teaches an interaural delay value (see fig.20 and col. 13 line 35-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Myers into the teaching of Nagata to

Art Unit: 2644

provide a binaural signal processing circuit and method which is capable of processing a signal so that a localization position of the sound can be selectively moved.

8. Claims 31 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata (US PAT. 5,974,154) in view of Platt (US PAT. 5,337,363), Gerzon (US PAT. 5,671,287) and Myers (US PAT. 4,817,149).

Consider claims 31 and 47, Nagata teaches that the switch circuitry comprises: an input switch (45,50) adapted to receive and forward the partially delayed digital audio signal to only the selected digital filter (621-62n); and an output multiplexer (61, 71) having a plurality of input ports and an output port, wherein: each input port is connected to a different digital filter (621-62n); and the output multiplexer (61, 71) is adapted to present the output from the selected digital filter at its output port (it has a chance by adjusting the state of switch matrix 45, the dials 41, 48 and 49 and the command switch 50 and see col. 4 line 60-col.5 line 67); the control module (65, microcomputer) comprises a LUT storing data that maps 3D positions to time delays; and the control module (65, microcomputer) is adapted to: receive a specified 3D position value; retrieve a corresponding time delay value from the LUT based on the specified 3D position value; and generate the first and second delay control signals on the time delay value (see col. 5 line 45-col. 6 line 61); but Nagata does not clearly teach that the buffer is a FIFO buffer adapted to receive a new digital value in the input digital audio signal at each clock cycle of the FIFO buffer; and the digital filters are all-pass filters having different phase shift values; and interaural delay value.

However, Platt teaches that the buffer is a first-in, first-out (FIFO) buffer adapted to receive a new digital value in the input digital audio signal at each clock cycle of the FIFO buffer (see col.9 line 20-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Platt in to Nagata to produce the sound being generated on a real time basis.

On the other hand, Gerzon teaches that the digital filters are all-pass filters having different phase shift values (see figs 23a-23c and col. 33 line 25-col. 34 line 48 and col. 42 line 5-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Gerzon into the teaching of Nagata to provide a pseudostereo or directional dispersion effect with both low phasiness and a substantially flat reproduced total energy response.

Mayer teaches an interaural delay value (see fig.20 and col. 13 line 35-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Myers into the teaching of Nagata to provide a binaural signal processing circuit and method which is capable of processing a signal so that a localization position of the sound can be selectively moved.

Response to arguments

9. Applicant's arguments with respect to claims 15-49 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2644

Conclusion

10. The prior art made of record and not relied upon is considered to applicant's disclosure. Lowe et al (US PAT. 5,105,462) is recited to show other related the method and apparatus for processing interaural time delay in 3d digital audio.

11. Any response to this action should be mailed to:

Mail Stop ____ (explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Facsimile responses should be faxed to:
(703) 872-9306

Hand-delivered responses should be brought to:
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lao,Lun-See whose telephone number is (571) 272-7501. The examiner can normally be reached on Monday-Friday from 8:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chin Vivian, can be reached on (571) 272-7848.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 whose telephone number is (571) 272-2600.

Lao,Lun-See
Patent Examiner
US Patent and Trademark Office
Knox
571-272-7501

Date 09-07-2005


VIVIAN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600